PRELIMINARY

2167
HIGH SPEED 16,384 x 1 BIT STATIC RAM

	2167-55	2167-70	2167L-70	2167-10
Max. Access Time (ns)	55	70	70	100
Max. Active Current (mA)	125	125	90	90
Max. Standby Current (mA)	40	40	30	30

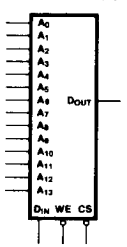
- 2141/2147 Upgrade
- Double Poly HMOS II Technology
- Completely Static Memory — No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Single +5V Supply
- Automatic Power Down
- 0.8–2.0V Output Timing Reference Levels
- High Density 20-Pin Package
- Directly TTL Compatible — All Inputs and Output
- Separate Data Input and Output
- Three-State Output

The Intel® 2167 is a 16,384-bit static Random Access Memory organized as 16,384 words by 1 bit. This memory is fabricated using Intel's high-density, high-performance technology—Double Poly HMOS II. This state of the art technology brings high-density to high-performance static RAMs. The design of the 2167 offers a 4x density improvement over the industry standard 2141 and 2147 with compatible performance. The 2167 offers the automatic power-down feature pioneered by the Intel 2147.

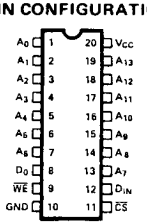
$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high (deselecting the 2167), the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 70% in larger systems where the majority of devices are deselected.

The 2167 is placed in a 20-pin package configured with the industry standard 16K x 1 pinout, offering the industry's highest density 16K static RAM. It is directly TTL compatible in all respects: inputs, output, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

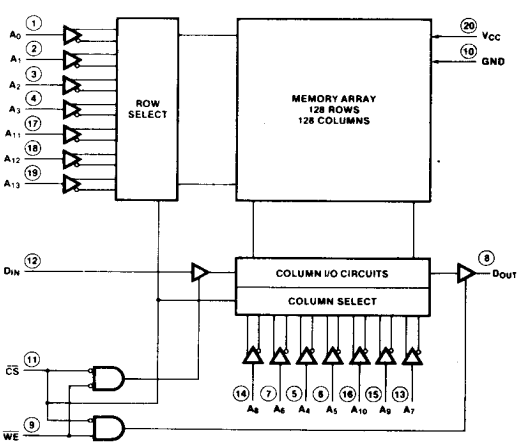
LOGIC SYMBOL



PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

A_0–A_{13}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
D_{IN}	DATA INPUT		
D_{OUT}	DATA OUTPUT		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

PIN	ADDRESS	FUNCTION
17	A_{11}	X_0
18	A_{12}	X_1
19	A_{13}	X_2
1	A_0	X_3
2	A_1	X_4
3	A_2	X_5
4	A_3	X_6
13	A_7	Y_0
7	A_6	Y_1
15	A_9	Y_2
6	A_5	Y_3
16	A_{10}	Y_4
5	A_4	Y_5
14	A_8	Y_6

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . −10°C to +85°C
Storage Temperature . . . . . −65°C to +150°C
Voltage on Any Pin With
Respect to Ground . . . . . −3.5V to +7V
Power Dissipation 1.2W
D.C. Output Current . . . . . 20 mA

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability*

D.C. AND OPERATING CHARACTERISTICS[1]

$T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise noted.

Symbol	Parameter	2167-55, 2167-70 Min.	Typ.[2]	Max.	2167L-70, 2167-10 Min.	Typ.[2]	Max.	Unit	Test Conditions
I_{LI}	Input Load Current (All Input Pins)		0.01	10		0.01	10	µA	V_{CC} = Max., V_{IN} = GND to V_{CC}
$\|I_{LO}\|$	Output Leakage Current		0.1	50		0.1	50	µA	$\overline{CS} = V_{IH}$, V_{CC} = Max., V_{OUT} = GND to 4.5V
I_{CC}	Operating Current		90	120		70	85	mA	$T_A = 25°C$; V_{CC} = Max., $\overline{CS} = V_{IL}$, Outputs Open
				125			90	mA	$T_A = 0°C$; V_{CC} = Max., $\overline{CS} = V_{IL}$, Outputs Open
I_{SB}	Standby Current		25	40		20	30	mA	V_{CC} = Min. to Max., $\overline{CS} = V_{IH}$
I_{PO}[3]	Peak Power-On Current		35	70		25	50	mA	V_{CC} = GND to V_{CC} Min., $\overline{CS}$ = Lower of V_{CC} or V_{IH} Min.
V_{IL}	Input Low Voltage	−3.0		0.8	−3.0		0.8	V	
V_{IH}	Input High Voltage	2.0		6.0	2.0		6.0	V	
V_{OL}	Output Low Voltage			0.4			0.4	V	I_{OL} = 8 mA
V_{OH}	Output High Voltage	2.4			2.4			V	I_{OH} = −4.0 mA

Notes:
1. The operating ambient temperature is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. Typical limits are at $V_{CC} = 5V$, $T_A = +25°C$, and specified loading.
3. A pull-up resistor to V_{CC} on the $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches I_{CC} active.

A.C. TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Level	1.5V
Output Timing Reference Levels	0.8–2.0V
Output Load	See Figure 1

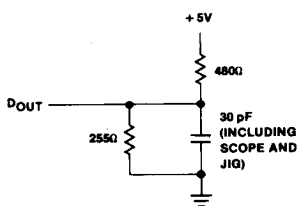


Figure 1. Output Load

CAPACITANCE[4]

$T_A = 25°C$, f = 1.0 MHz

Symbol	Parameter	Max.	Unit	Conditions
C_{IN}	Input Capacitance	7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	6	pF	V_{OUT} = 0V

Note: 4. This parameter is sampled and not 100% tested.

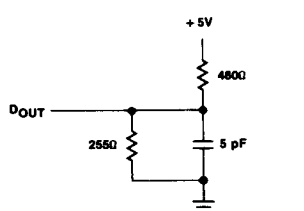


Figure 2. Output Load for t_{HZ}, t_{LZ}, t_{WZ}, t_{OW}

A.C. CHARACTERISTICS

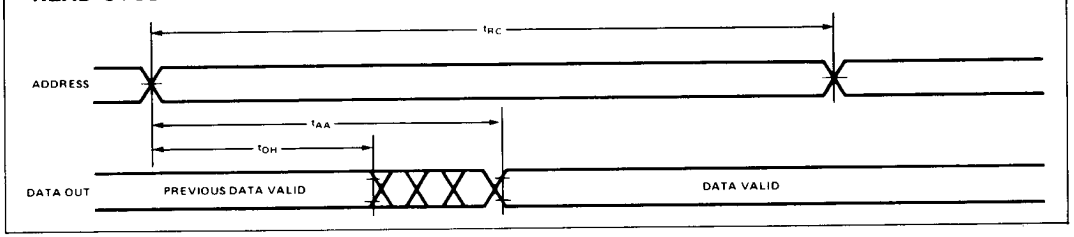
$T_A = 0°C$ to $70°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise noted.

READ CYCLE

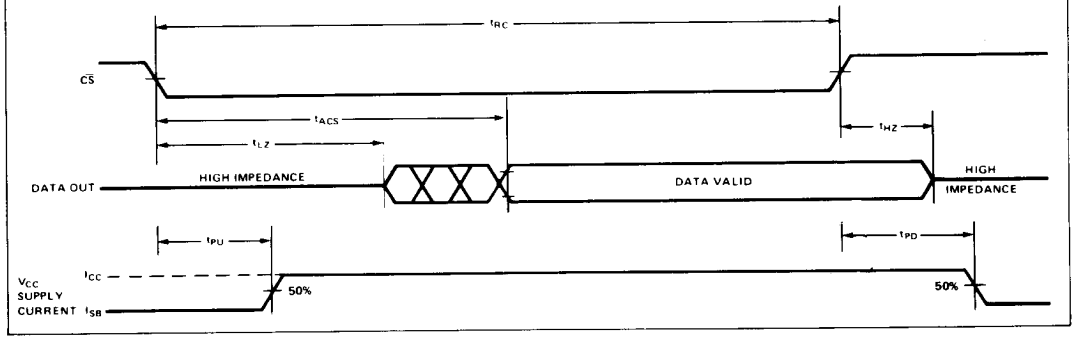
Symbol	Parameter	2167-55 Min.	2167-55 Max.	2167-70, 2167L-70 Min.	2167-70, 2167L-70 Max.	2167-10 Min.	2167-10 Max.	Unit
t_{RC}[1]	Read Cycle Time	55		70		100		ns
t_{AA}	Address Access Time		55		70		100	ns
t_{ACS}	Chip Select Access Time		55		70		100	ns
t_{OH}	Output Hold from Access Change	5		5		5		ns
t_{LZ}[2,3]	Chip Selection to Output in Low Z	10		10		10		ns
t_{HZ}[2,3]	Chip Deselection to Output in High Z	0	30	0	40	0	40	ns
t_{PU}	Chip Selection to Power-Up Time	40		50		55		ns
t_{PD}	Chip Deselection to Power-Down Time		55		70		80	ns

WAVEFORMS

READ CYCLE NO. 1 [4,5]



READ CYCLE NO. 2 [4,6]



Notes:
1. All Read Cycle timings are referenced from the last valid address to the first transitioning address.
2. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
3. Transition is measured ± 500 mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.
4. $\overline{WE}$ is high for Read Cycles.
5. Device is continuously selected. $\overline{CS} = V_{IL}$.
6. Addresses valid prior to or coincident with $\overline{CS}$ transition low.

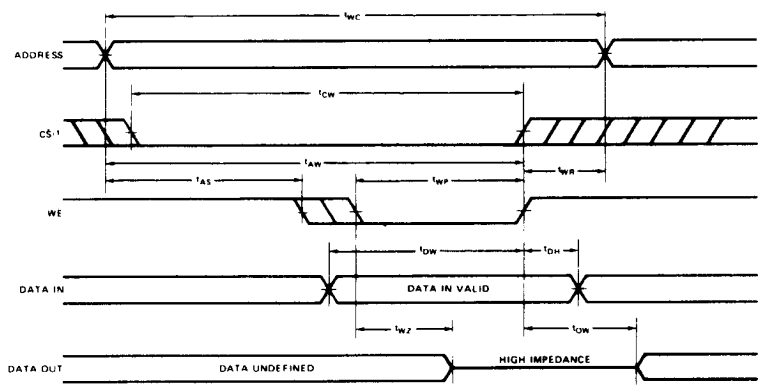
A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

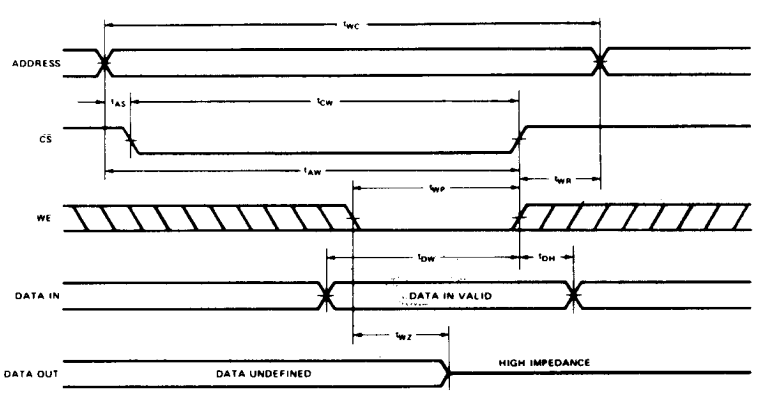
Symbol	Parameter	2167-55 Min.	2167-55 Max.	2167-70, 2167L-70 Min.	2167-70, 2167L-70 Max.	2167-10 Min.	2167-10 Max.	Unit
t_{WC}[2]	Write Cycle Time	55		70		100		ns
t_{CW}	Chip Selection to End of Write	55		70		90		ns
t_{AW}	Address Valid to End of Write	55		70		95		ns
t_{AS}	Address Setup Time	0		0		5		ns
t_{WP}	Write Pulse Width	35		40		45		ns
t_{WR}	Write Recovery Time	0		0		5		ns
t_{DW}	Data Valid to End of Write	25		30		35		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{WZ}[3]	Write Enabled to Output in High Z	0	25	0	35	0	35	ns
T_{OW}	Output Active from End of Write	0		0		0		ns

WAVEFORMS

WRITE CYCLE #1 ($\overline{WE}$ CONTROLLED) [4]



WRITE CYCLE #2 ($\overline{CS}$ CONTROLLED) [4]



Notes: 1. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
3. Transition is measured ±500 mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.
4. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.